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Field Effect Transistors(FETs) and Silicon Controlled Rectifier(SCR).

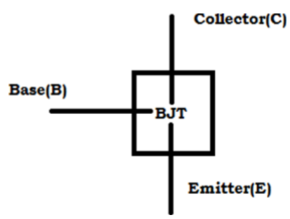
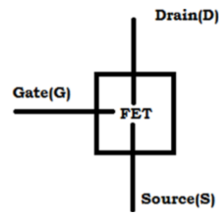
1. FETs:

FET is an acronym for the field-effect transistor. The FETs are three-terminal unipolar devices and conduction will be controlled by the electric field. Hence FETs are also called Field controlled/Voltage controlled devices.

1.1. Similarities between BJTs and FETs.

- Both are transistors.
- Both have two junctions and three terminals. Both are controlling the conduction of current and
- Both are semiconductor devices.

1.2. Difference between BJTs and FETs.

Sl. No.	BJTs	FETs
1		
2	Two Types • NPN(**N**ever **P**oints i**N**) • PNP(**P**oints i**N** **P**ermanently)	Two Types • N-Channel(points i**N**) • P-Channel(**P**oints out)
3	$I_C = f(I_B)$ i.e., $I_C = \beta I_B$	$I_D = f(V_{GS})$ i.e., $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

4	Collector Current is approximately equal to Emitter Current. $I_C \cong I_E$	Drain Current is equal to Source Current. $I_D = I_S$
5	Current Controlled Device	Voltage Controlled Device

6	Current conduction takes place by both holes and electrons. Hence Called Bipolar Transistors.	Current conduction takes place by only the majority charge carriers, either electrons or holes. Hence Called Unipolar Transistors.
7	Poor Thermal Stability	Good Thermal Stability
8	Low Input impedance	Very High input impedance
9	High Power Consumption	Low Power Consumption
10	Occupies More Space in a circuit	Occupies less space, hence can be fabricated easily in Integrated Chips.
11	**High Gain***	**Low Gain***
12	**Large Bandwidth***	**Bandwidth is low***

*Disadvantages of FETs over BJTs.

1.3. Classification of FETs.

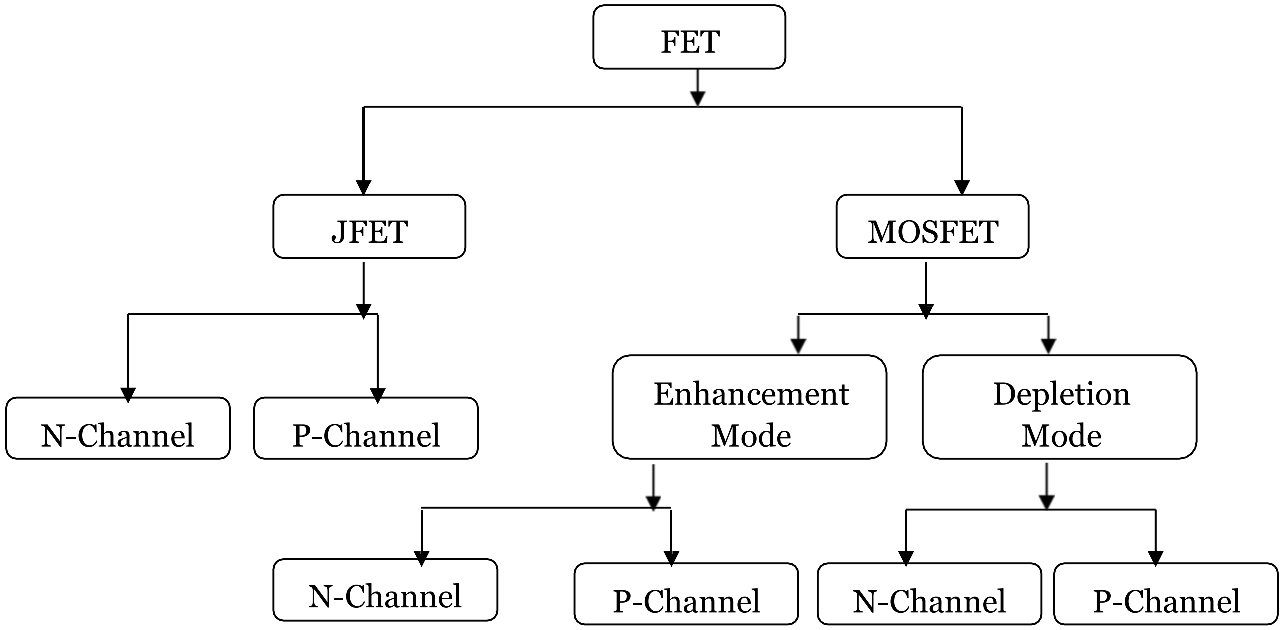


Figure 1.1: Classification of FET

N-channel and P-channel JFETs, Construction, Working principles, and Characteristics are discussed in the present context.

Analogy for discussing the working principle of JFETs:

A spigot/tap will be the best analogous system for JFET. Consider a tap shown in figure 1.6.

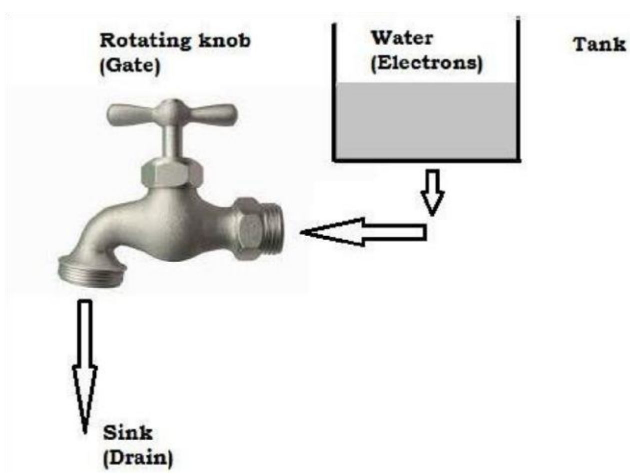


Figure 1.6. Analogous system for N-JFET.

Figure 1.6., shows a spigot/tap, in which the water will flow from the tank to the sink, and it will be controlled by rotating the controlling knob. Similarly in JFETs, the electrons will move from the source terminal to the drain terminal and will be controlled by the gate terminal. If the volume of the water in the tank is more, water movement will be faster, and more could be collected at the sink, similarly if the drain to source voltage increases, more electrons will drift from the source terminal to the drain terminal and causes a conventional current from drain to the source terminal, called as drain current.

Now consider a rotating knob of tap, that will be rotated to block the flow of water, but assume that it does not block completely. And due to more pressure of water flow from the tank, there should be a constant amount of water will flow. If the further increasing the pressure of water flow from the tank, the controlling element in a tap is going to damage, and more current will flow.

Similarly in JFET, if the pinch-off condition occurs, the constant current will flow from drain to source, which is due to the increase in drifting of electrons towards the drain terminal or due to high current density (conventional current will flow in opposite direction to the movement of the electrons). This occurs at

$V_{DS}=V_P$ (Pinch-off Voltage). If $V_{DS}>|V_{VBD}|$, Junction will break and the device will get damaged.

1.4. N-Channel JFET.

In the N-channel Junction field-effect transistor, N-type material is the major part and the electrons are majority charge carriers, the current conduction takes place by these majority charge carriers.

1.4.1. Construction:

Starting with a large piece of N-type semiconductor material, it acts as a channel and two small pieces of P-type Semiconductor materials are embedded in the two sides of the N-type material, forming two PN Junctions shown in figure 1.2. The Major portion in the structure is the N-type semiconductor material and it is between the two P-type semiconductor materials that create an N-channel, hence called as N-Channel JFET.

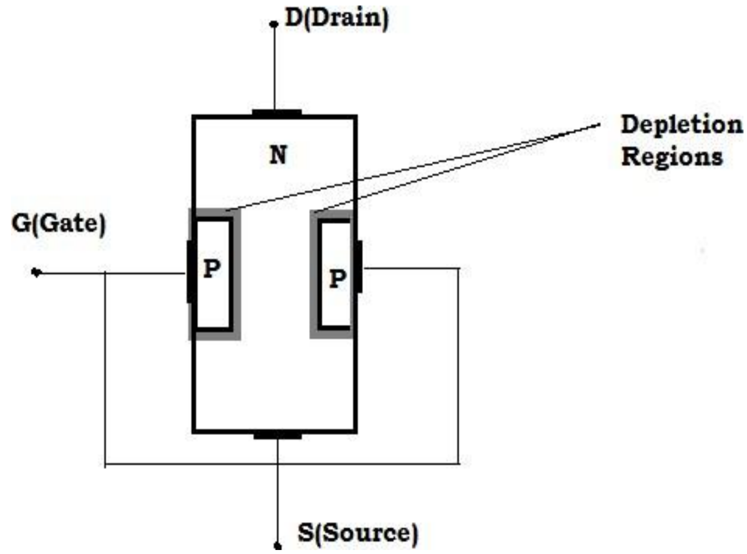


Figure 1.2: Structure of the N-Channel JFET.

The metallic contacts are deposited on the sides of the structure to connect the electrodes. The upper electrode is denoted as D and it is called as Drain terminal, the bottom electrode is denoted as S and it is called as Source terminal, the other two sides are internally connected and denoted as G and it is called as Gate terminal, shown in figure 1.2.

The N-Channel is having electrons that are majority charge carriers and holes are minority charge carriers, similarly, P-type materials are having holes that are majority charge carriers and electrons are minority charge carriers. Under normal room temperature, without bias, the electrons from the channel tend to move from N-type to P-type and vice-versa creates a small depletion region shown in figure 1.2.

1.4.2. Working Principle:

The working of N-Channel JFET will be discussed in two cases, as follows.

Case I: V_{GS}=0(Zero Gate Biasing) and V_{DS}>0V(Positive Voltage).

Case II: V_{GS}<0(Negative Biasing) and V_{DS}>0V(Positive Voltage).

1.4.2.1. Case I: VGS=0(Zero Gate Biasing) and VDS>0V(Positive Voltage).

The N-Channel JFET is Biased with a positive voltage between Drain to Source and Zero Biasing between Gate to source as shown in figure 1.3.

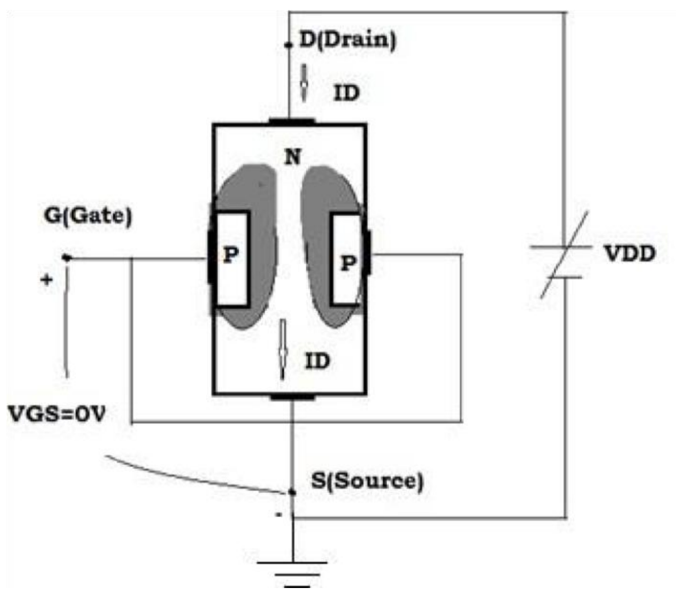


Figure 1.3. Under Positive Drain voltage and zero gate voltage.

By increasing the Positive voltage V_{DD}, the depletion region increases in the form of wedge shape shown in figure 1.3., because the PN Junction near the Drain terminal is reverse biasing and near the source terminal is forward biasing, hence the depletion region near the drain terminal is more compared to near the source terminal.

The shape of the depletion region is further explained in detail with the following analogy. The channel is like a resistor and considers there are five equal valued resistors are connected in series between drain to source shown in figure 1.4., suppose the applied voltage is 5 Volts, the voltage drop across each resistor is 1V.

With respect to A, the voltage is 1V, at B 2V, at C 3V, and at D 4V, i.e., the Positive voltage at D is more positive than C, at C is more Positive than B, and so on. Hence the width of the depletion region is more near the drain terminal compared to the Source.

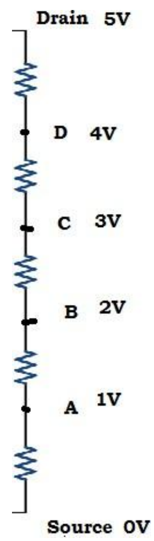


Figure 1.4. Showing Analogy for Channel.

If V_{DD} is increasing, the area and width of the channel decreases, hence less drain current will flow through the channel from drain to source, if V_{DD} is further increased to a level, which touches both the depletion regions(not overlapping) and it is called Pinch-Off. The voltage(positive voltage applied between drain to source) at which, the depletion regions are going to the Pinch-off condition, is called Pinch-off voltage shown in figure 1.5.

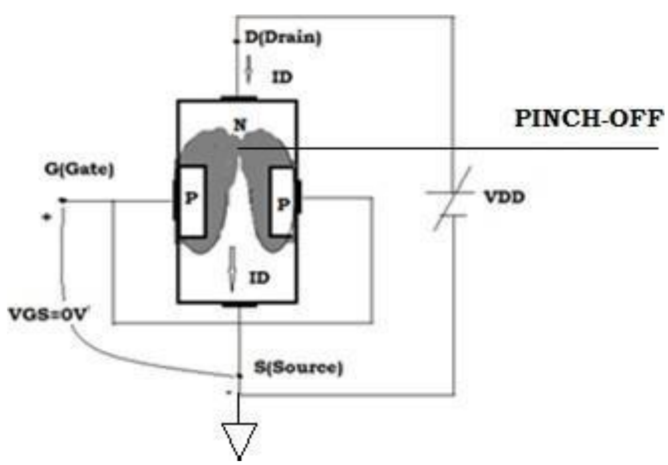


Figure 1.5. Pinch off condition

At Pinch-off condition, the constant current will flow from drain to source, because at pinch-off the depletion regions will touch but it will not create a barrier to move electrons from source to drain, and also due to high current density.

The output characteristic of N-Channel JFET is shown in figure 1.7.

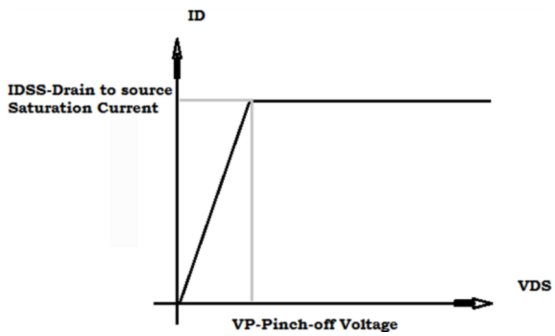


Figure 1.7. Output characteristics of N-channel JFET, with VGS=0 and VDS>0V.

1.4.2.2. Case II: VGS<0(Reverse Biasing) and VDS>0V (Positive Voltage).

The N-channel JFET's drain terminal is biased with positive voltage i.e. VDS=+ve, and the gate terminal is biased with negative voltage i.e., VGS=-Ve, shown in figure 1.8. In this case, the pinch-off condition occurs quite earlier and is decided by the negative potential applied at the gate

i.e. more negative the V_{GS}, earlier the pinch-off, reducing I_{DSS} shown in the output characteristics, refer figure 1.9. As the phenomenon continues, it is seen that a condition arises wherein the saturation level of the drain-to-source current occurs right for a value of 0 mA. This means the current doesn’t flow through the device and essentially the device will turn OFF. The value of V_{DS} for which this happens will be nothing but the negative pinch-off voltage i.e. $V_{DS} = -V_P$.

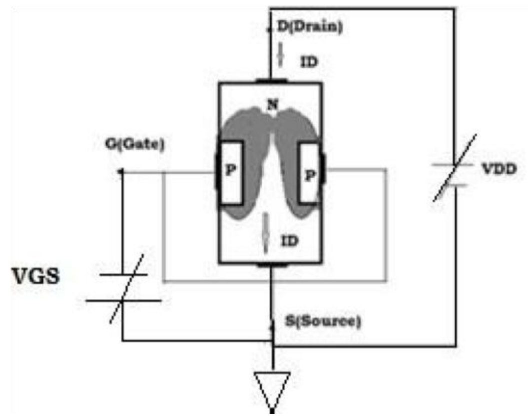


Figure 1.8: Forward biasing DS and Reverse biasing GS.

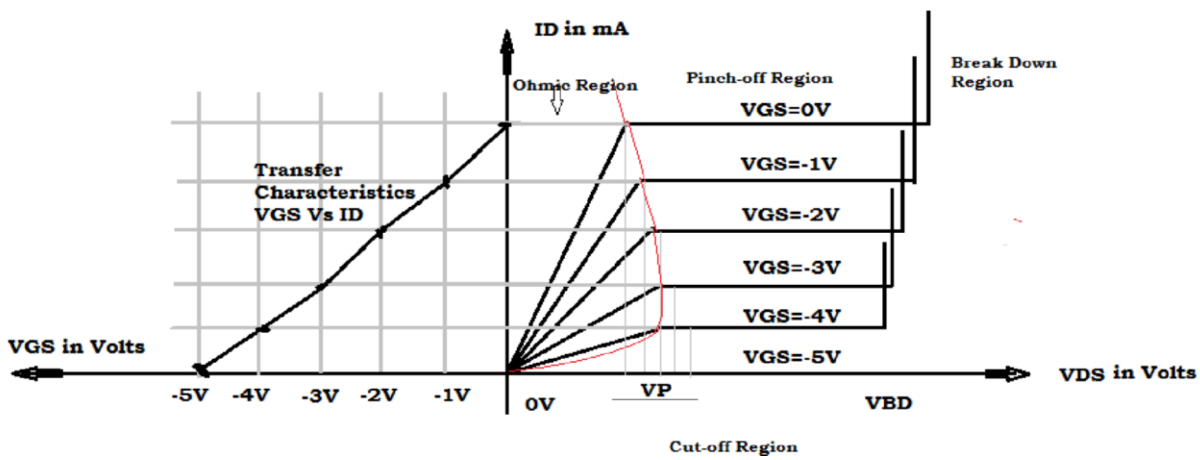


Figure 1.9: Drain and Transfer Characteristics of N-channel JFET.

Note: Students are informed to analyze the working principles of P-channel JFET.

2. SCRs:

SCR is an acronym for Silicon Controlled Rectifier.

- The device which converts ac to dc or the device which conducts current only in the forward direction is called rectifier/Diode.
- If the diode is made up of silicon material, then the diode is called a silicon diode/silicon rectifier. The silicon material is used instead of Germanium because of the requirement of high temperature to handle high currents and power.

- If the silicon diode is controllable, then the device is called a silicon-controlled diode/silicon-controlled rectifier.

Hence, the SCRs are defined as the devices which conduct current in the forward direction and also controllable and are made up of using silicon material. These devices have three junctions, three terminals, and four layers.

2.1. Basic Structure of SCR.

The basic Structure of SCR is shown in figure 2.1, which consisting of four layers, its four layers are arranged as PNPN. The outer layers are connected to terminals to form a positive terminal called an Anode, a Negative terminal called a Cathode, and a terminal from P-Layer nearer to the cathode called a Gate.

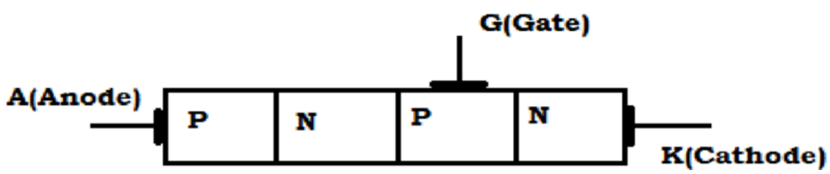


Figure 2.1: Basic Structure of the SCR

2.2. Circuit symbol.

The circuit symbol of SCR is shown in figure 2.2, the terminals anode, cathode, and gate are shown. I_A is Anode Current, I_G is the gate current, which is applying to control the anode current during the forward bias.

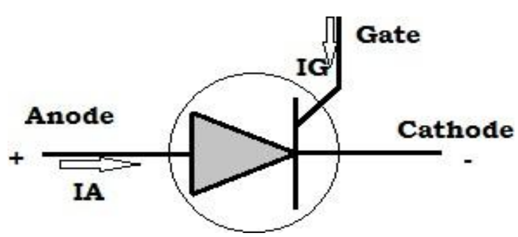


Figure 2.2: Circuit Symbol of SCR.

2.3. Working Principle.

Silicon Controlled Rectifiers begin their conduction during the forward bias, the forward biasing arrangement shown in figure 2.3. That is Positive terminal of the battery is connected to the anode terminal and the negative terminal of the battery is connected to the cathode terminal.

The working principle of SCRs can be analyzed using two cases.

Case I: Without Gate signal(V_G=0 and V_{AA}>0).

Case II: With Gate signal(V_G>0 and V_{AA}>0).

2.3.1. Case I: Without gate signal(V_G=0) and V_{AA}>0.

When the SCR is under forward biasing and without the gate signal, as shown in figure 2.3. The junctions J_1 and J_3 are forward biased and J_2 is reverse biased. Hence conduction path does not exist. During this condition, the device acts as an open circuit even under forward biasing.

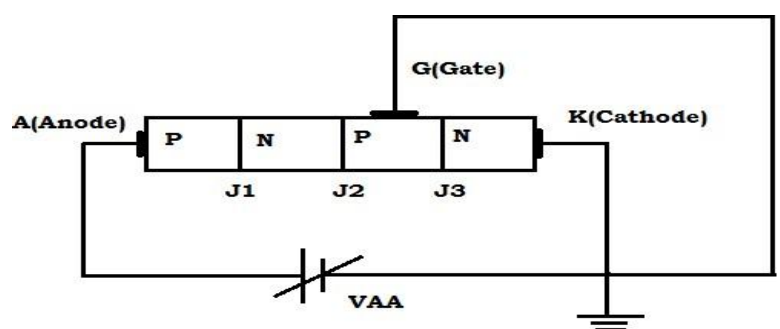


Figure 2.3: Forward Biasing of SCR without Gate Signal.

2.3.2. Case II: With Gate signal(V_G>0) and V_{AA}>0.

When a gate signal(Generally positive Clock Pulse) is applied along with forward biasing of SCR shown in figure 2.4. The gate current I_G(sufficiently large enough to drive the device) flows into the gate terminal and hence the junction J_2 gets forward biased along with J_1 and J_2, then the device goes to conduction mode and the current will flow from anode to cathode terminal. During this condition, the device acts as a short circuit/ON switch.

The silicon-controlled rectifiers, forward current offers a very low resistance of 0.01 to 0.1Ω, whereas it offers infinite resistance under non-conduction mode.

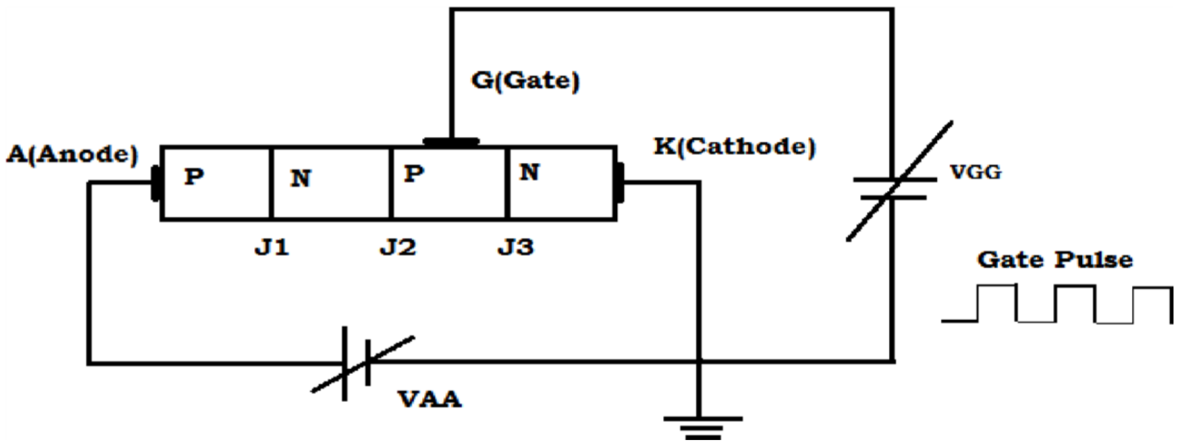
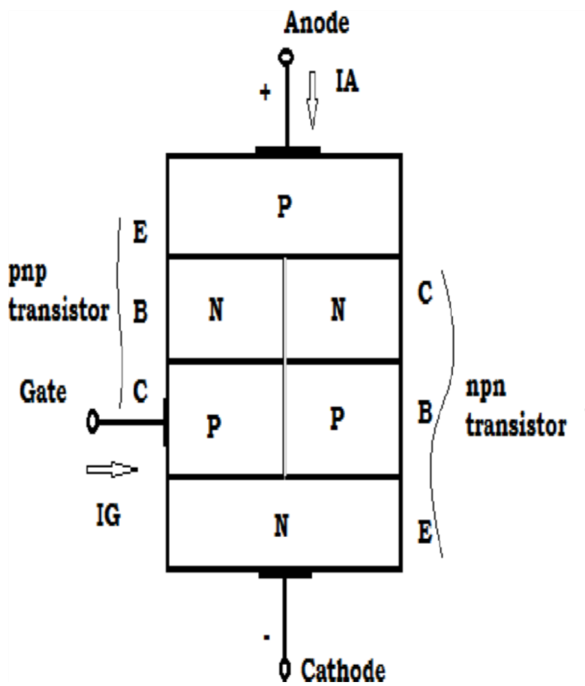


Figure 2.4: Forward Biasing of SCR with Gate Signal.

During forward biasing and with gate signal, all the junctions J_1, J_2, and J_3 are forward biased and regenerative action takes place. Because of regenerative action, even after removing the gate current, the device will not be turned off. Hence, an External circuitry/Commutation process is used to turn off the SCRs.

2.4. Two Transistor model or Analogy of SCR.

The two-transistor model of SCR is shown in figure 2.5. The four layers of SCR are divided into two transistors by subdividing the middle N and P Layers. The cross-sectional view of SCR is shown in figure 2.5(a) and the equivalent circuit using BJT symbols is shown in figure 2.5(b).



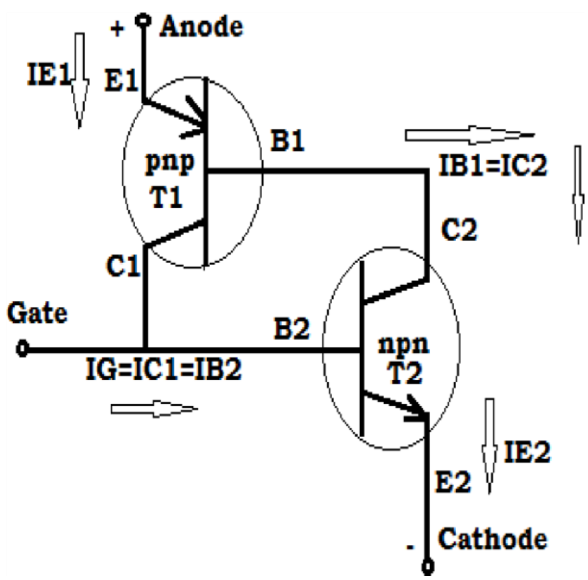


Figure 2.5(a): Cross sectional view. Figure 2.5(b): Transistor equivalent circuit.

Figure 2.5: Two Transistor model of SCR.

From the above diagrams, it is observed that the four layers of SCR are comprised of two transistors, one NPN and another PNP. As there is electrical continuity between the two transistors, the base of the T_1 is connected to the Collector of T_2; and the collector of T_1 is connected to the base of T_2 is shown in figure 2.5b.

2.4.1. Switching action

Case-I: Without gate signal(V_G=0) and V_{AA}>0.

Gate(C_1/B_2) and Cathode(E_2) are connected to the ground terminal, i.e., the zero gate bias. Let a positive voltage V_{AA} be applied to the anode(E1). With V_G=0, the V_{BE2}=0 so, the CB junction of T_2 is reverse biased, and only leakage current(I_{CO}) will be supplied to the base of T_1. It is too small to turn on the transistor T_1. Thus both T1and T_2 are in the off state. Refer to figure 2.6.

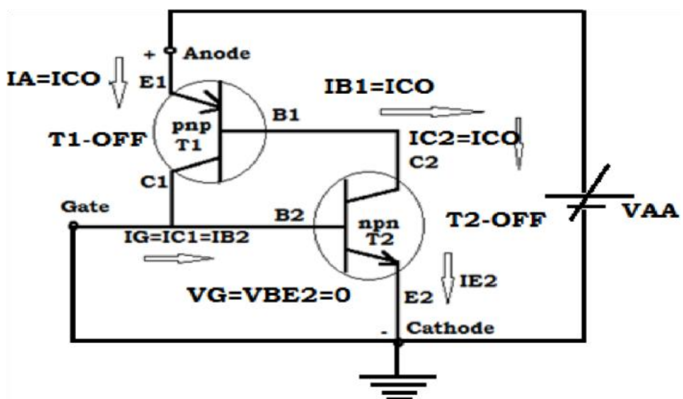


Figure 2.6: Showing Working principle of SCR under VG=0.

so anode current is given by, $I_A=I_{B1}=I_{CO}$ is of negligible quantity. That is SCR is in the turn-off state. means SCR acts as an Open Circuit or Open Switch.

Case-II: With Gate signal(V_G>0) and V_{AA}>0.

Let a Positive voltage V_G be applied at the gate terminal(C_1/B_2). As $V_{BE2}=V_G$, and on making V_G sufficiently large, I_{B2} will cause T_2 to turn on and the collector current I_{C2} becomes large. As $I_{B1}=I_{C2}$, T_1 turns on causing a large collector current $I_{C1}(I_A=I_{C1})$ to flow. This in turn increases I_{B2} causing a regenerative action to set in (this is indeed positive internal feedback). Refer to figure 2.7.

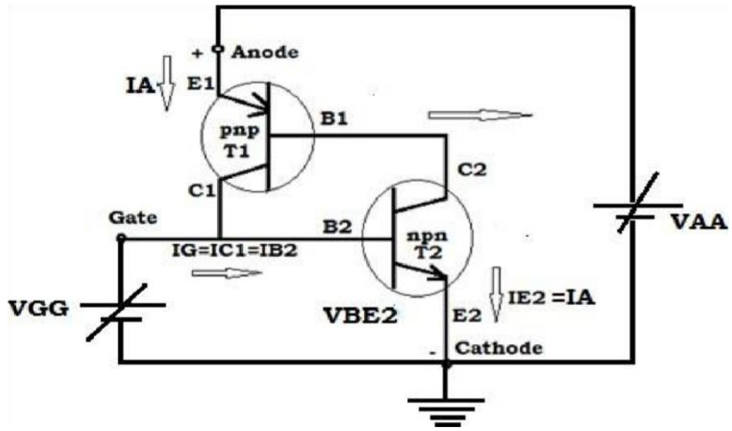


Figure 2.7: Showing Working principle of SCR under VG>0.

so anode current is given by, $I_A=I_{E1}=I_{E2}$ is of maximum current. that is SCR is led to turn-on. i.e., SCR acts as a short circuit or closed switch.

2.4.2. Commutation.

As observed from the switching action of SCR, once the SCR is turned on, due to regenerative action, the SCR always remains in ON condition, thus Commutation circuits/mechanisms are required to turn off the SCR.

Commutation is a process of turn-off the SCR, there are two types of commutation

- Natural Commutation
- Forced Commutation.

2.4.2.1. Natural Commutation.

The AC signal is fed to the SCR, when the signal passes through zero shown in figure 2.8, the current becomes zero, in that situation the SCR turns off naturally. This type of turning off the SCR is called natural commutation and also called line commutation.

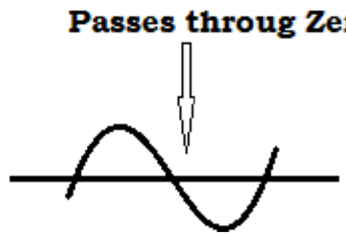


Figure 2.8: Signal Passes through Zero.

2.4.2.2. Forced Commutation.

Forced commutation is a process of turn-off the SCR, through an external circuit. In this case, the current through the SCR is forced to become zero by passing a current through it in opposite direction from the external circuit.

There are many types of forced commutation, in the present context, a simple series combination of the transistor and a dc battery is discussed to turn off the SCR as shown in figure 2.9.

To turn off the SCR, a positive I_B pulse of magnitude, large enough to drive the transistor into the saturation level is applied at the transistor base. the transistor acts as a short circuit. This causes the flow of very large I_{off} through the SCR in opposite direction to its conduction current.

The total SCR current reduces to zero in a very short time causing SCR to turn off.

Turn off time of an SCR is typically 5-30µs.

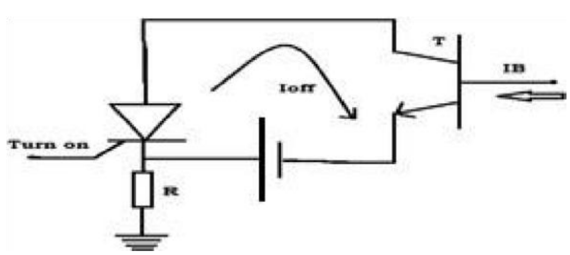


Figure 2.9: Turn-off Circuit

2.5 SCR Characteristics.

when the positive voltage $V_{AK}=V_F$ is applied between Anode to the cathode. Without a gate signal, a small leakage current will flow from anode to cathode due to minority charge carriers, which is negligibly small and considered as an OFF state. The voltage drop across the SCR is the same as the applied voltage, during the OFF state.

When a gate pulse is applied, the SCR will turn on, once the SCR turns on the voltage across the SCR i.e., V_{AK} drops to the threshold voltage level(Vt=0.7V, because Silicon controlled rectifier) and current suddenly increases. Further increase in V_F causes an increase in I_A but Voltage remains constant. The Plot of V_{AK} vs I_A is shown in figure 2.10 for different values of I_G.

If the forward break-over voltage V_F is small, more gate current is required to trigger the SCR.

The SCRs will trigger even without a gate signal if the voltage across the SCR exceeds V_{BD}(Break down voltage, practically very high voltage level).

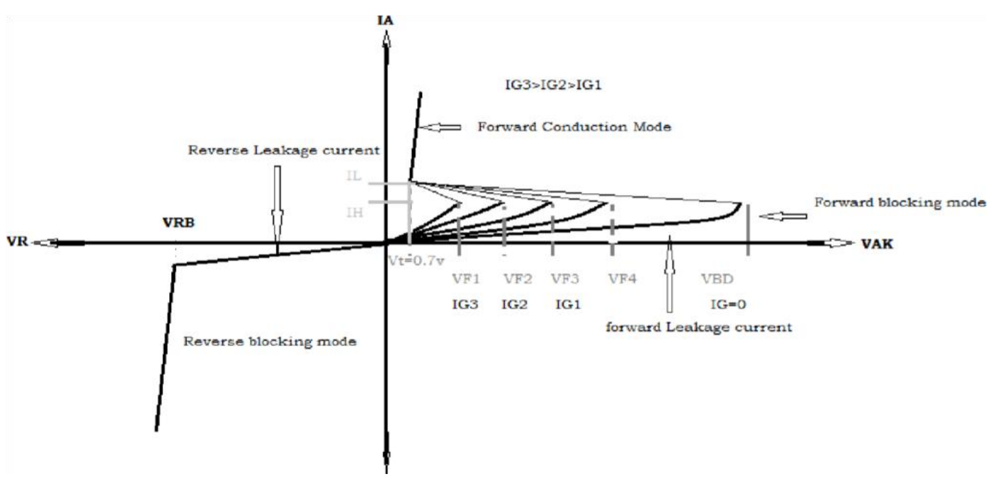


Figure 2.10: VI Characteristics of SCR.

2.5.1. Terminologies used in SCR and its characteristics.

a. Forward break-over voltage(VF)

Forward break-over voltage is the voltage at which for a given IG, the SCR enters into conduction mode. This voltage reduces as I_G increases.

b. Holding Current(IH)

Holding current is the value of the current below which SCR switches from conduction mode to forward blocking mode(OFF mode).

c. Forward and Reverse blocking

Forward and Reverse blocking regions are those regions in which the SCR is open-circuited and no current flows from anode to cathode.

d. Latching current(IL)

Latching current is the minimum anode current above which gate losses its control.